Accelerating Technology Development Through the Use of Stone Pillar TestPlanManager for Improved Test Algorithm Management and Automated Test Plan Generation

Generating test plans for parametric device characterization involves the creation, management and application of complex algorithms that can include numerous dependencies on device geometric parameters, operating voltage, temperature and other factors. This paper explores improvements to this process implemented by a first tier semiconductor company and customer of Stone Pillar Technologies, for analog technology development through the use of Stone Pillar TestPlanManager (TPM) for automated test plan generation and management.

Parametric Test Plan Creation's High Cost, Complexity

Algorithm creation for technology development is an ongoing area of research. This is especially true for analog and mixed-signal applications where the increasing complexity of circuit models demands an increasing number of measured parameters. It also demands a detailed understanding of the underlying device physics to correctly measure the required parameters. Device parameters, and the way they are measured, can be a function of device geometry, operating voltage, operating temperature and numerous other factors. The engineer developing the testing strategy must factor in each of these considerations to in order to correctly characterize the device.

These considerations dictate the complexity of the algorithms and the scaling of algorithms into test procedures. In addition, the number of devices needed to characterize an analog/mixed-signal process, especially during early stage technology development, is immense. The management of test chip details, algorithm application and the resulting

measured parameters constitutes a data management problem that requires a different set of skills from those required to optimize algorithm implementation.

Test chips that cover thousands of device variations need to be combined with algorithms scaled for each device instance. Results from one test may serve as inputs to subsequent tests or as Boolean determinants of which subsequent tests should be run on a particular device. The required algorithms must be selected, scaled into fully specified procedures, applied to the devices of interest, connecting to details about terminals and die location. Following the test execution, results must be organized and analyzed to find one or more devices to target for use in designs or to determine desired characteristics from processing or geometric splits.

This process is usually managed as a combination of complex coding in the control language of the tester, coupled with manual or database-driven control of all of the various inputs to the test system. This process requires an engineer with detailed knowledge of the algorithms, the device details and the management of the test data. Unfortunately, it is prone to errors and often requires multiple contributors to perform the required tasks.

As a result, highly-skilled device test experts often spend their time on tedious control language implementation and debugging. This reduces the time available for higher priority activities for which their skills are better suited, such as developing new algorithms, refining or optimizing existing ones or analyzing test results.

The Goal: Faster, More Efficient Creation of Parametric Test Plans

The customer's analog technology development group recognized an opportunity in this dilemma. If the creation of test plans could be automated in a way that permitted the test algorithms to be scaled based on the device geometric parameter values, they could be

written in a general form. And, the work of creating the test plan could be reduced to a simple drag and drop operation.

They had several objectives when making the decision to automate the test plan creation:

- Speed the creation of test plans. Test plans for a leading edge analog/mixed-signal process require the scaling of algorithms and application of these to hundreds or thousands of device variations. The desired solution should exploit details about the test chip already available to reduce the amount of input required by a user to apply tests to the devices. In short, the user should be able to drag and drop tests onto devices, apply tests across all or single device instances, and do so with a minimum of manual intervention.

- Reduce errors in test plan creation. Errors in test plan creation are costly to diagnose and can result in incorrect conclusions. The desired system should reduce errors and provide traceability from result to procedure to algorithm and work back to layout. Reducing errors would allow engineering resources to be focused on algorithm development and data analysis, and away from tedious debugging and documentation interpretation tasks.

- Improve management and re-usability of test algorithms. Provide a way to allow algorithms created for one technology to be applied across other technology families and the ability to save and retrieve implementations of procedures from one technology or test chip iteration for reuse in the next.

- To create a standard for test program methodology, algorithm use and test reuse that could be deployed across multiple test locations around the world.

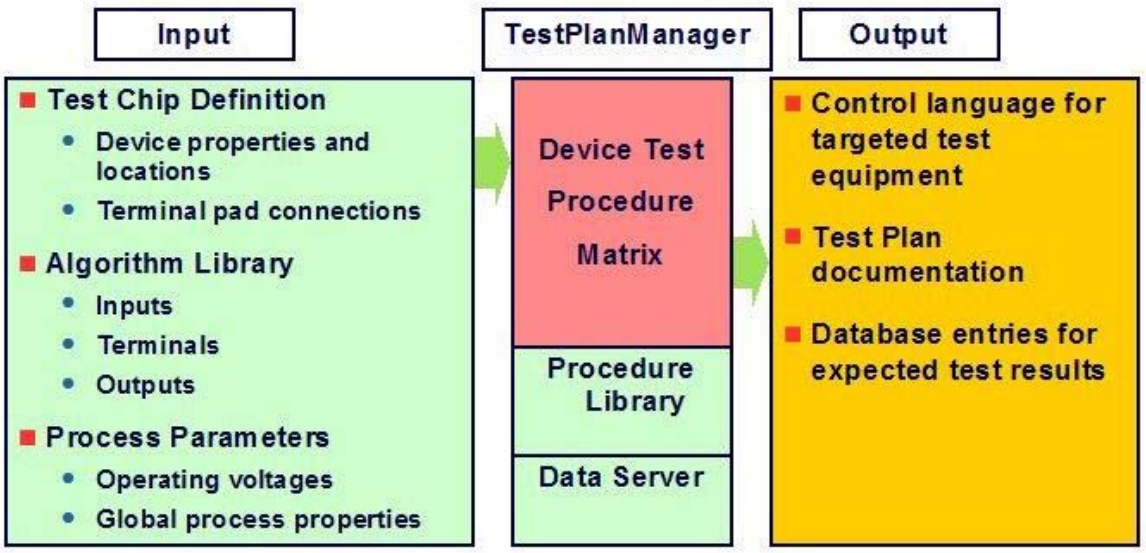
The Solution: An Automated System for Test Plan Generation

The solution developed in close collaboration with Stone Pillar Technologies, is an automated software system called TestPlanManager (TPM) that is built around the detailed representation of the test chip. It includes full details of geometric variations, pad module location, device location within the pad module, and module positions within a test chip or test die. It also includes management capabilities that allow test algorithms, with unspecified values for inputs such as biasing or temperature, to be scaled into test

procedures. These test procedures fully specify input values based on available information about test structures included in the test chip or the specific process technology that might specify global information.

In order to create a scalable algorithm, the engineer responsible for test development inserts variables during test generation, such as “emitter area” or “temperature” or inline math expressions that are automatically filled with actual values.

Figure 1 shows inputs available within the test plan development software and results.

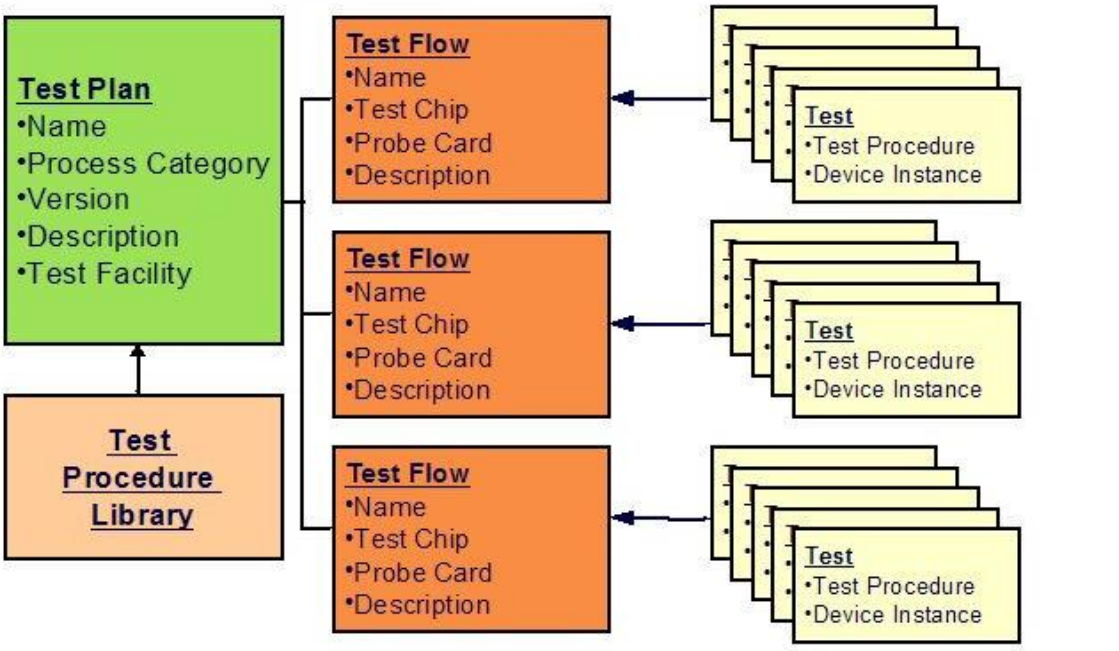


Error-prone, manual implementation of parameters for each device test is replaced by the automation provided by TestPlanManager. By bringing together the details of the test chip and scalable algorithms, test plan creation is reduced to a drag and drop operation. Graphical user interface (GUI) capabilities of TPM apply dozens or hundreds of tests across thousands of devices, shielding the user from device-specific details.

Tests can be grouped and applied as a group or individually and keyed to results of

previous tests. This is managed through GUI capabilities that automatically create test control language and confirm the required test order, further eliminating errors.

Figure 2 shows the algorithms, procedures and flows that comprise a complete test plan.



Structuring these elements allows maximum re-usability and allows for the creation of procedures that can be applied across a wide variety of device variations or operating conditions.

The automation eliminates the need for users to have detailed knowledge of the tester control language or the algorithm implementation to create test plans. Instead, users simply select from a library of scalable algorithms that is set up by an expert user. The speed with which test plans can be generated makes it possible to create a range of test plans, some for performing a survey of a range of devices. Others can be used to perform detailed testing of devices that might be justified for only a small fraction of the testing due to time constraints.

Furthermore, since TPM is tester-independent, it can generate output for different target test environments from the same test plan definition, providing flexibility for re-targeting different test hardware from the same test development environment.

Complex analog/mixed-signal processes that require large numbers of test structures gain from the improved efficiency of automatic test plan generation. Even with a few devices, there can be benefit, in test plan generation speed, consistency and management. TPM also provides the ability to review or modify test plans and test chip details to create new or modified test flows.

This approach has reduced the time for test plan creation within the customer's analog technology development group from days to hours, a savings of approximately 75%. Entire test plans can be assembled in a single session of less than two hours, instead of taking several sessions over several days.

According to the customer, “Using Stone Pillar TestPlanManager, we now have the flexibility to set up and modify a range of test plans from sparse to complete and ensure that all of these are synchronized with any algorithm updates. Procedure management capabilities allow the our team to store, scale and apply test procedures for a range of technologies. In addition, errors in the test plans, which previously took a significant effort to analyze and debug, have been eliminated. Our team now spends more time working on algorithm development and optimization, such as enhancing adaptive testing, instead of keying in and debugging repetitive tester code.”

In addition to time savings and increased flexibility, errors have been reduced and traceability makes it easy to confirm whether observed phenomenon are the result of algorithmic anomalies or valid device characteristics.

Conclusion

By automating the generation of test plans, the customer was able to reduce the engineering cost of test plan generation, improve algorithm reuse, reduce errors and improve traceability. The improved processes saved engineering resources, reduced errors and improved test debugging efficiency, and improved test quality. The ease of use of TPM eliminates the need by new test engineers to learn the tester control language. Instead, they can be trained to use the GUI-driven software and produce test plans immediately. In the future, this methodology will enable device engineers to design their own test plans.

The customer recognized the importance of automating testing to assure product quality and has made this a key objective. Using Stone Pillar TestPlanManager, they have been able to standardize their test program methodology, algorithm use and test reuse for leading edge technology development. Based on the success of this approach, the customer has deployed the methodology and the use of Stone Pillar TestPlanManager across multiple test facilities throughout the world.

###